SI/PI Simulation Technologies for High-Speed Design

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Keywords Signal integrity, Power integrity, EMC, High-speed, Low-voltage.

Abstract

Due to recent rapid progress of Large-Scale Integration (LSI) technology for electronic circuits, there has been a dramatic improvement in the performance of electronic equipment.

Due to the development of high-speed, high-frequency, and low- voltage for electronic equipment, there is a concern regarding various noises that had not been a design issue previously, but may cause malfunction of the electronic equipment.

To meet customer requirements, we constantly produce high quality products by emphasizing the importance of analyzing problems and taking proper measures during the initial design stage of the overall product development cycle.

Signal Integrity (SI)/Power Integrity (PI) simulation has been frequently applied during the design stage in order to reduce the Turn-Around Time (TAT) to achieve a more expedient time to market.

1 Preface

Due to the higher speed of the interface like a Double Data Rate (DDR) memory, it has become difficult to accurately transmit signals from the driver to the receiver of the Integrated Circuit (IC) (see Fig. 1.). In addition, the allowable noise margin of the power supply has been reduced as a result of ever-improving high performance and low-voltage tendency for the high-speed digital ICs (see Fig. 2.). Nowadays, utilizing the conventional design approach based on past experiences and intuition cannot effectively solve Signal Integrity (SI) and Power Integrity (PI)-related issues. Fig. 3 shows technical challenges relating to SI and PI.

Due to increasing processing speed and lowering of core voltage, Printed Circuit Board (PCB) design has become more than a challenging task. The market constantly demands a reduction of product development time and overall cost reduction (see Fig. 4.). To solve such issues, we are making full use of circuit simulation like SI/PI analysis starting from the upstream stage of product development. This is in order to realize optimum noise

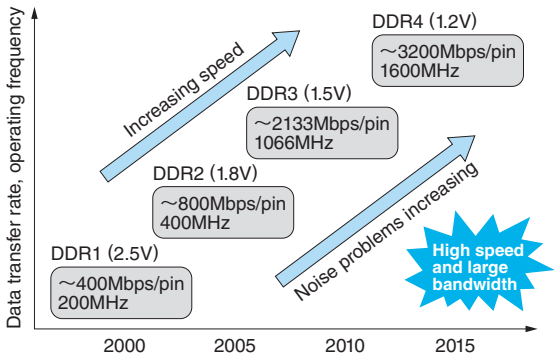

Fig. 1 Issues Due to High Speed

As the clock frequencies increase, SI problems such as timing delay, reflection, and crosstalk become critical.

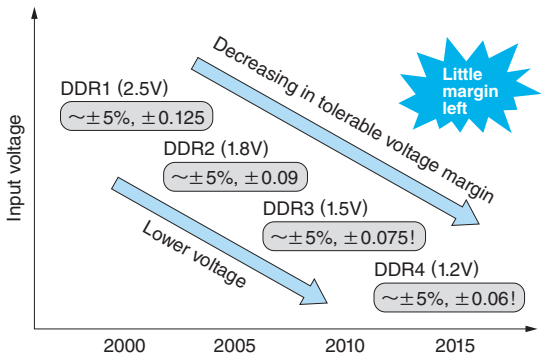

Fig. 2 Issues Due to Low Voltage

Low core voltage causes PI problems such as an increase in plane impedance and voltage drop become critical.

elimination and establish various specifications. In this manner, we are providing high-quality products to our customers. In order to tackle such issues, we brought in SI/PI simulation technologies during the initial design stage of product development. We ran through a series of design optimization and specification review, and eventually produced high quality products on schedule.

This paper briefly explains our SI/PI simulation technologies during initial design stage of product development.

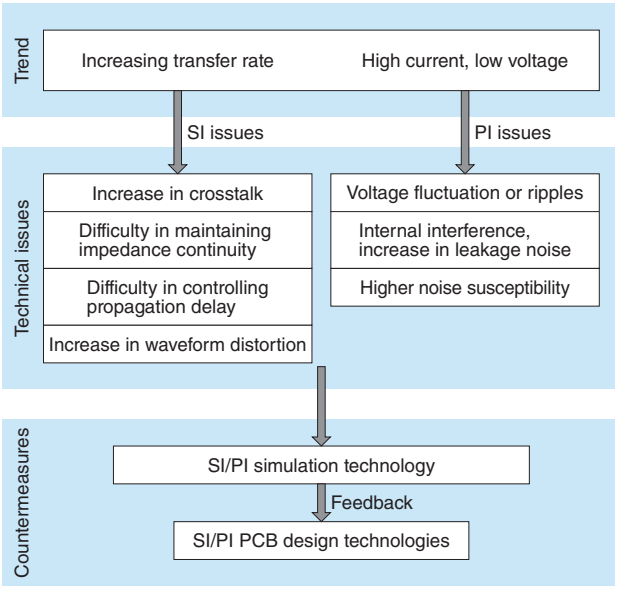

Fig. 3 Technical Issues on SI and PI

Technical issues and measurements are shown. This is due to higher speed and lower voltage.

2 SI/PI Simulation

2.1 SI Simulation

Fig. 5 shows the topology of SI simulation. PCBs, connectors, and other high-speed transmission lines are carefully modeled in order to maintain

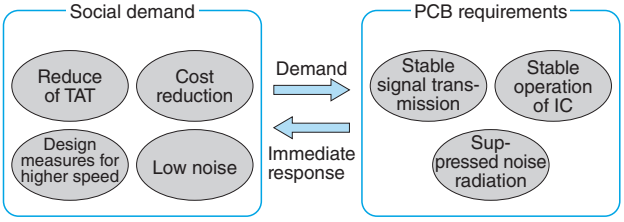

Fig. 4 Requirements and Measures

PCB development items according to the customer and market demands are shown.

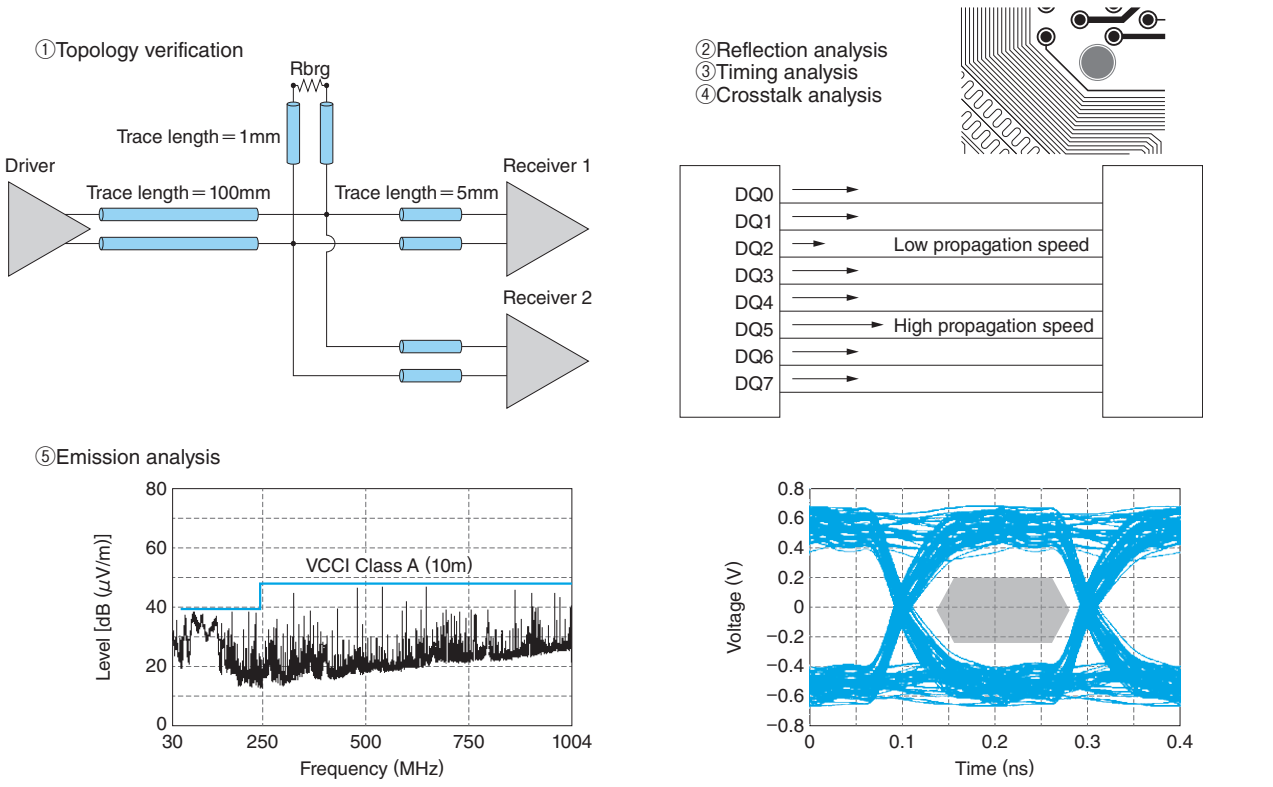

Fig. 5 SI Simulation

SI simulation is required to ensure the integrity of the transmission line. This approach is actively used as a supporting tool for the elimination of problems such as timing delay, reflection, and crosstalk.

signal integrity (integrity of the signal waveform) between the driver and receiver.

We could also identify a potential noise problem of the PCB by carrying out SI simulation. Early counter-measures could also be carried out immediately. There are four main points for SI simulation:

(1) Topology design

Before routing, timing analysis is performed in order to seek optimal topology (characteristic impedance, routing path, trace length, noise reduction components).

(2) Reflection analysis

Analysis of reflection due to impedance mismatch is carried out, which includes the phenomena of propagation delay, and overshoot/undershoot and ringing of signals.

(3) Timing analysis

This analysis verifies correct circuit operation at a specific speed as requested by the circuit designer.

(4) Crosstalk analysis

This analysis evaluates the coupled noise between adjacent traces.

(5) EMI Emission analysis

Analysis of potential sources of radiated noise among high-speed signals.

2.2 PI simulation

Fig. 6 shows the contents of PI simulation. Impedance of the Power Delivery Network (PDN) from voltage regulator module to the pads on the IC chip has been analyzed. The impedance is kept within the specified range in order to reduce voltage fluctuation that might cause IC malfunction. A noise elimination design approach by PI analysis is applied to the PCB design so that low-noise products with stable power sources can be produced. PI simulation is comprised of four categories as follows:

(1) DC analysis

Analysis of IR drop caused by DC current and resistance of power plane in the PCB (essential to ensure the voltage drop is within IC specification)

(2) Input impedance※1 (Z11) simulation

Analysis of input impedance of the power delivery network between Power and GND plane as

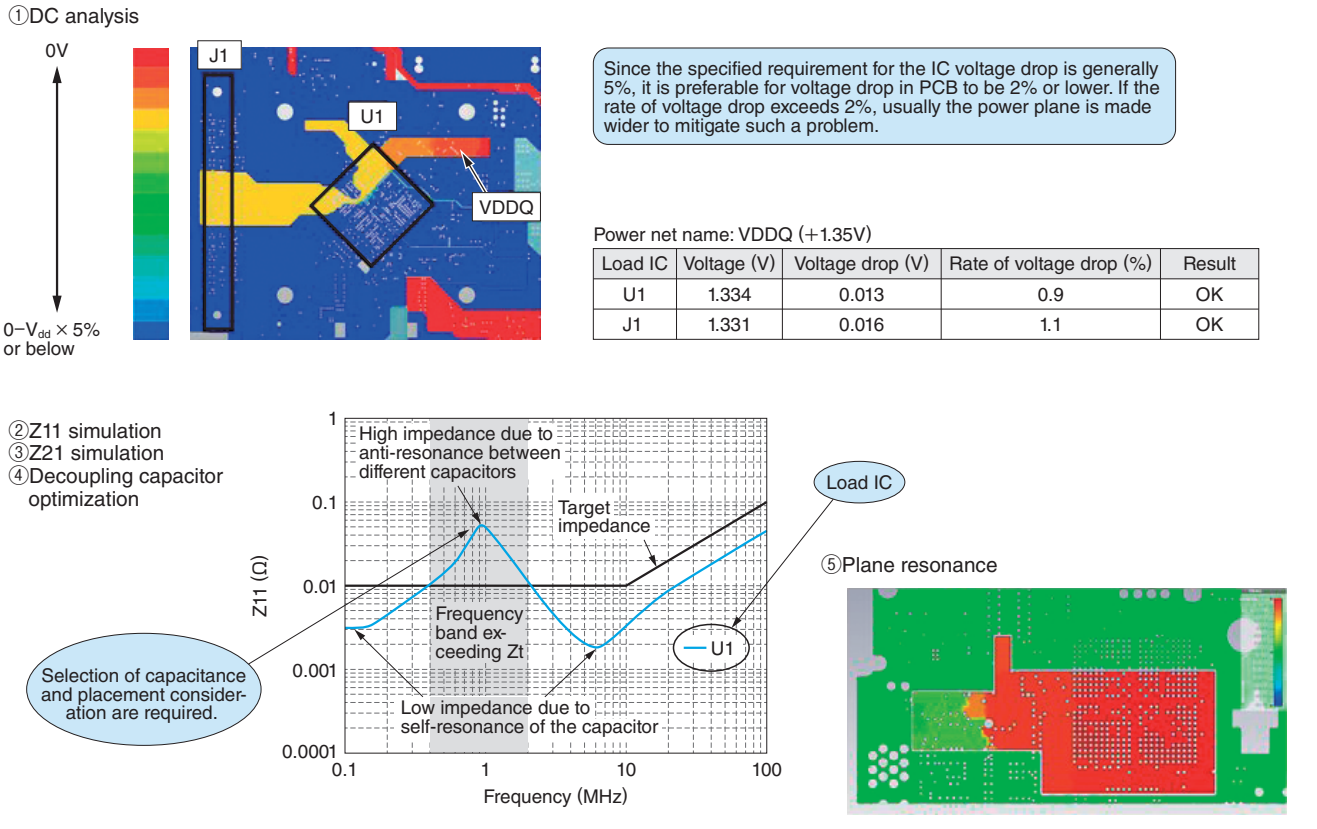

Fig. 6 PI Simulation

PI simulation is required to ensure the integrity of the PDN. This approach is actively used as a supporting tool for the elimination of problems such as impedance rising in power planes and subsequent voltage drops.

seen from the IC.

(3) Transfer impedance※2 (Z21) simulation

Analysis of the conducting noise from noisy IC to other ICs, connectors or cables.

(4) Optimization of decoupling capacitors

Optimization of the quantity, capacitance, etc. of decoupling capacitors in order to keep the PDN impedance below the target impedance※3 determined from total output current and allowable ripple voltage.

(5) Plane resonance simulation

Resonance analysis in order to identify the location where voltage drop becomes larger (resonance) as a result of multiple reflections within the plane pair (Power-Power, or Power-GND) due to the coupling of energy to the plane pair from the adjacent route.

3 Postscript

This paper introduced the necessity for SI/PI simulation and related activities. Reworked cycles due to SI and PI problems could be reduced by applying SI/PI simulation technologies during the initial design stage where potential problematic spots could be filtered out. As a result, we are able to efficiently offer high-quality products to our customers.

We established a sophisticated measure in suppressing conducting noise due to PDN by using simulation technologies. In the near future, we are going to develop the technologies for suppressing emitted noise. This technology also benefits the analysis of the malfunction of the equipment due to the coupling of radiated electromagnetic waves from surrounding equipment.

(Notes)

※1. Input impedance: Dominant for assessing PI.
(1) Input impedance of the power delivery network of the IC.
(2) PDN impedance as seen from the load IC.
(3) The lower the impedance, the less power noise.

※2. Transfer impedance: Parameter related not only to PI but also to EMI.
(1) EMI noise coupling characteristics of the PDN behaving as an antenna.
(2) Noise propagation characteristics observed from noise source to other chips, connectors, and board edge.
(3) The lower the impedance, the less the propagation efficiency of power noise.

※3. Target impedance: Maximum allowable value of the impedance of the PDN across a range of specified frequencies.